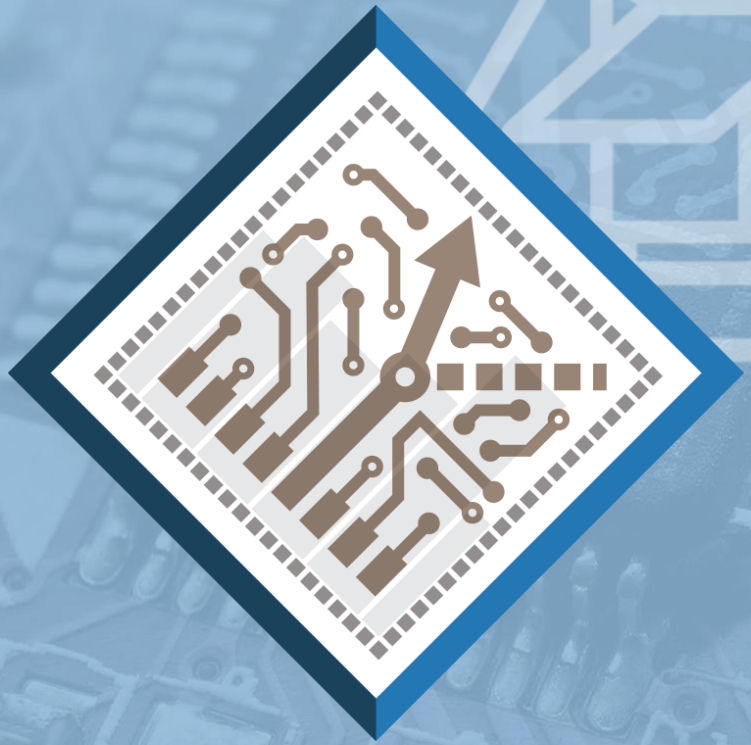
# THE ELECTRONICS RESURGENCE INITIATIVE



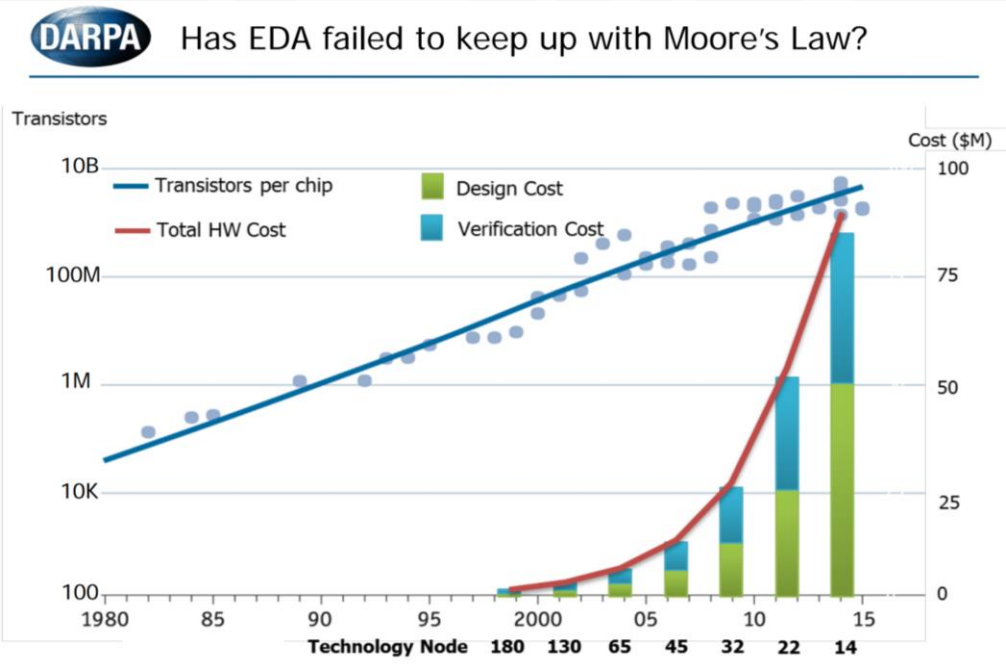
# OpenROAD: Foundations and Realization of Open, Accessible Design

# Andrew B. Kahng

UC San Diego

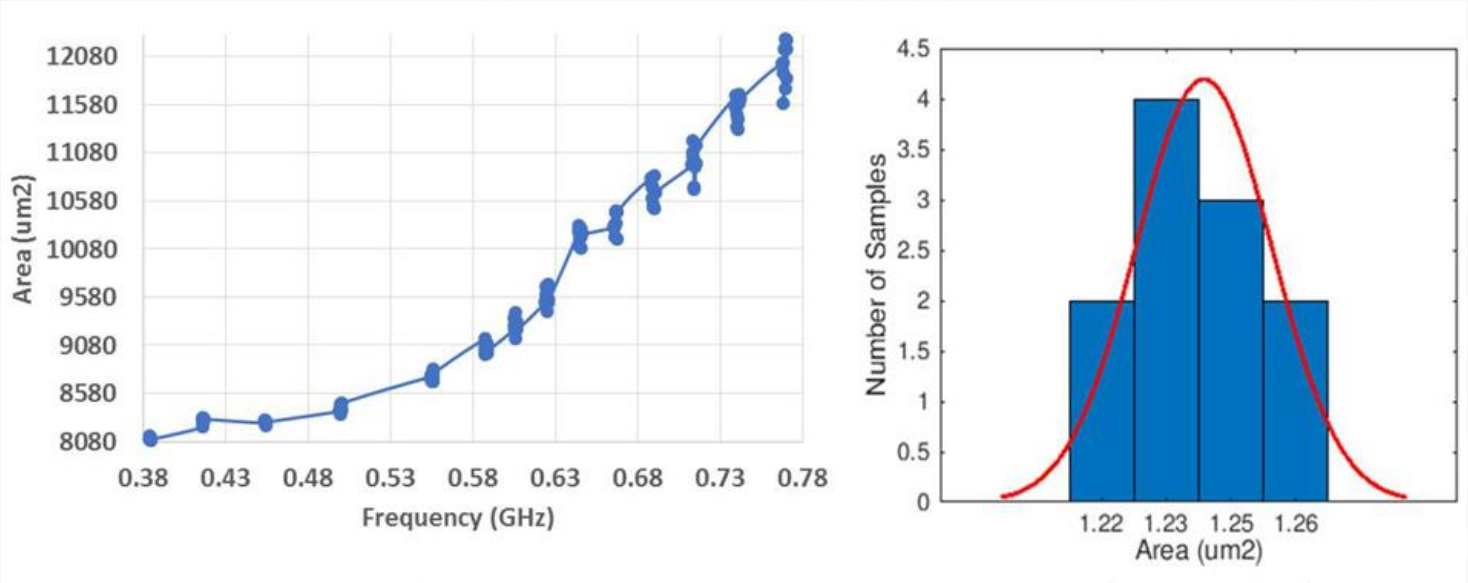
# THE DESIGN CHALLENGE

- Enormous barriers to hardware design in advanced technologies: Cost, Expertise, Unpredictability

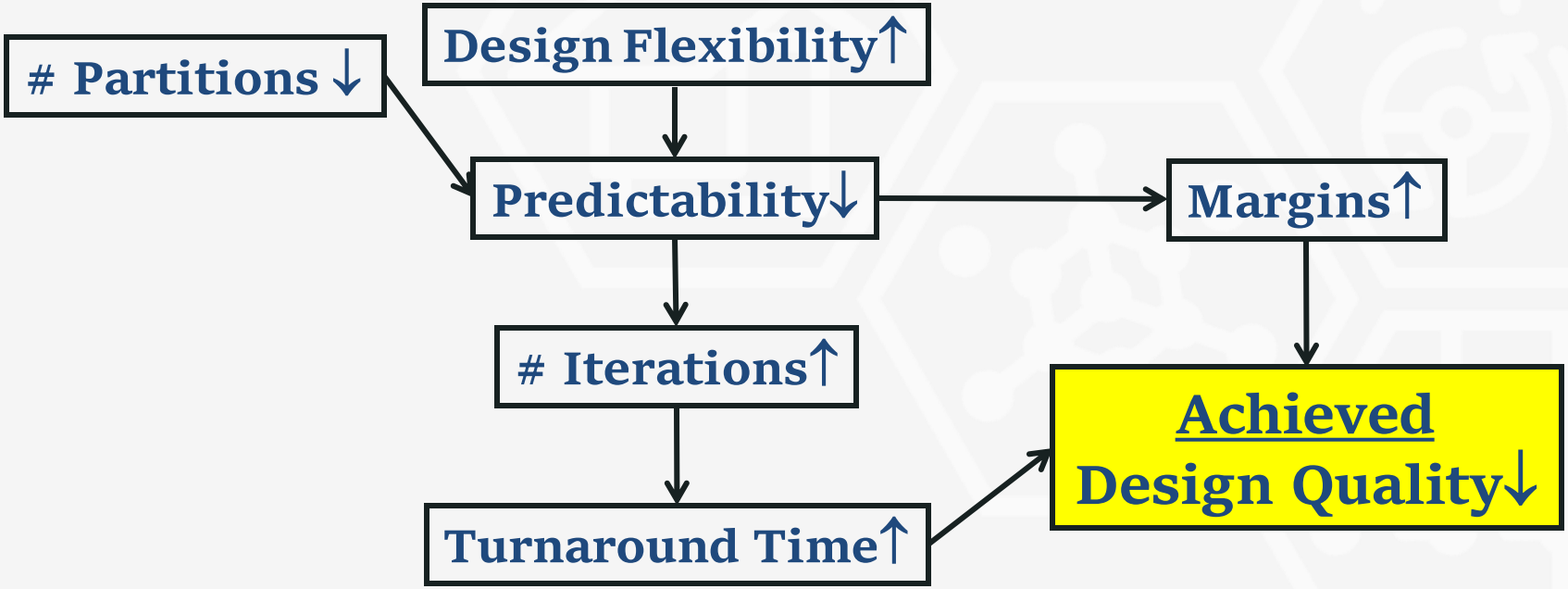


# HOW IS IT DONE TODAY?

- Hardware design tools have evolved into complex "Swiss army knives"
- Chaos when tools are forced to "try hard"



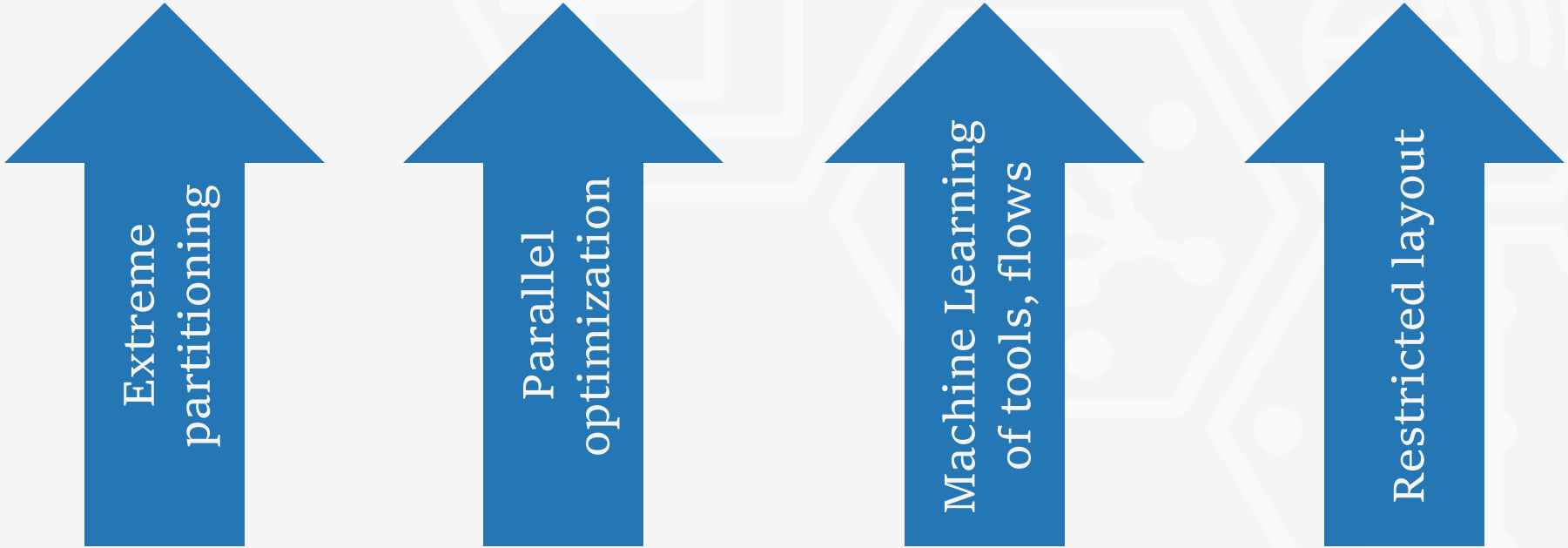
# "LOCAL MINIMUM" OF HW DESIGN




**Today: in a "local minimum" of design technology, methodology, and quality**

# NEW IN OUR APPROACH

**24 hours, no humans – no PPA loss**

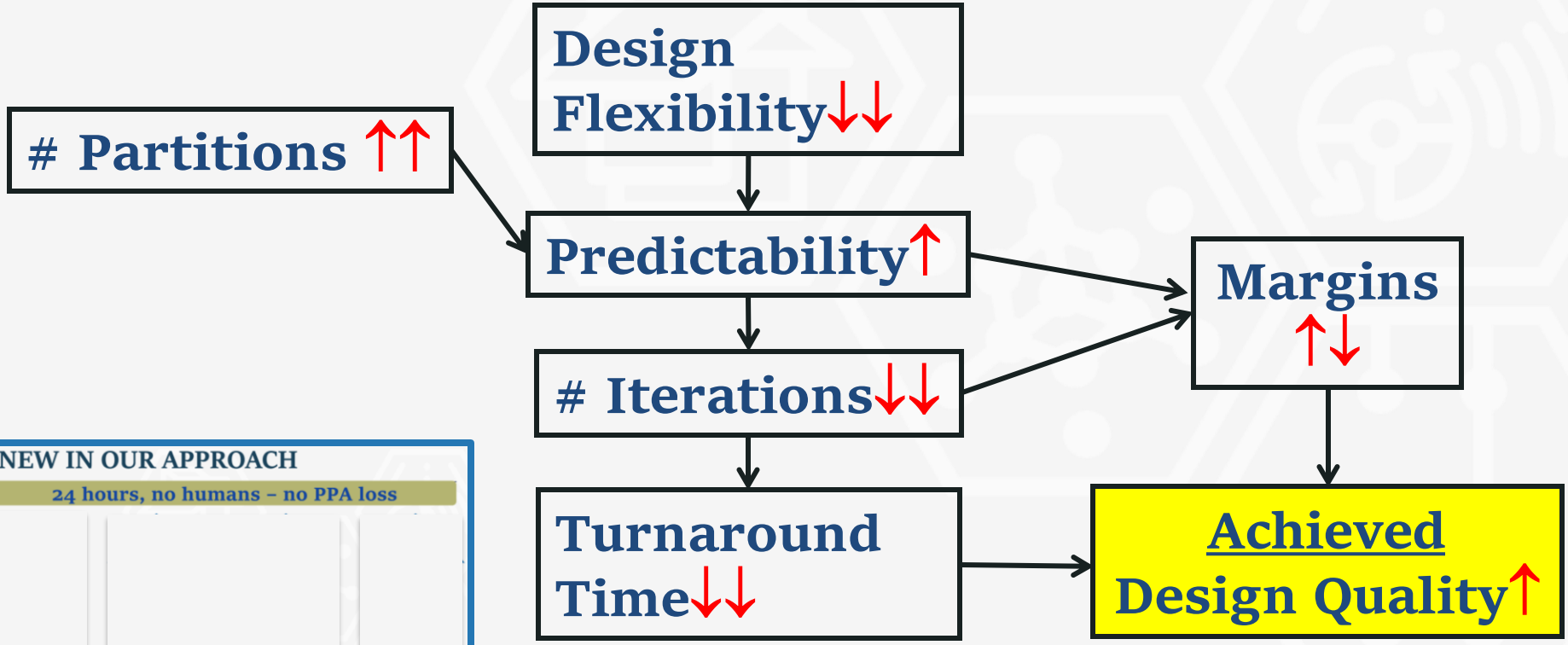



**Design Complexity**

# FOUNDATIONS OF OUR APPROACH

- No Humans: tools must adapt and self-tune, must never get stuck unexpectedly
- 24 hours: extreme partitioning of problems
  + parallel search on cloud
  + machine learning for predictability
- Mantra: Correctness and safety by construction
- Mantra: Embrace freedom from choice

# A NEW DESIGN PARADIGM



# TECHNICAL CHALLENGES

- Data: small and expensive!
- Humans: are in the loop for good reasons!
- Fundamental tradeoffs: analysis cost vs. accuracy, optimization effort vs. quality
- Activation energies: new sharing mindsets, open-source ecosystem

# OUR GOAL

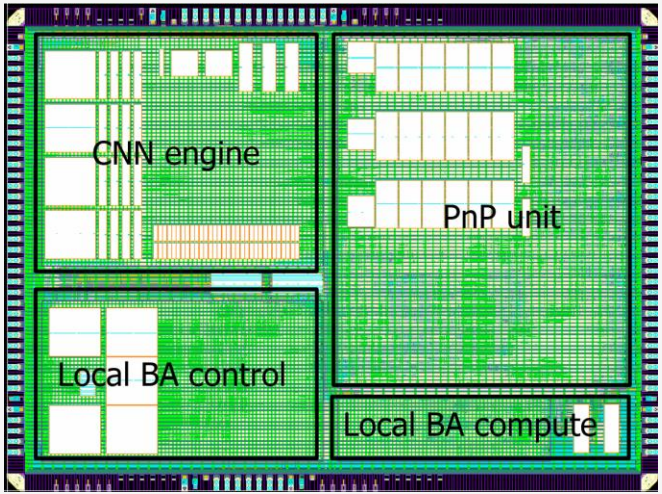
- 24-hour, No-Human-In-Loop layout design for SOC, Package and PCB with no Power-Performance-Area (PPA) loss
- Tapeout-capable tools in source code form, with permissive licensing → seed future “Linux of EDA”

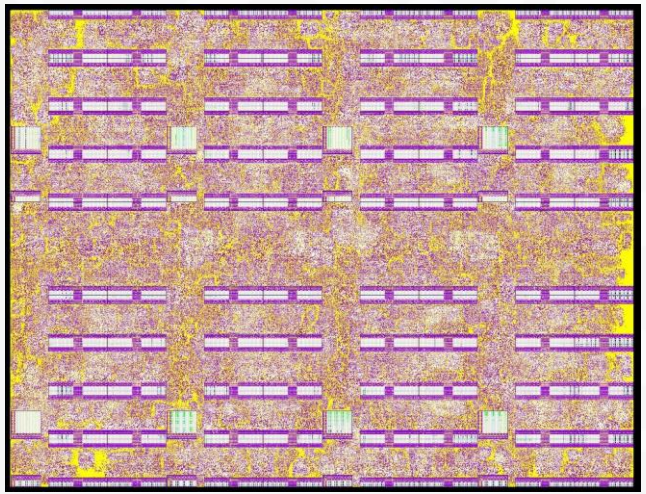
# IMPACT IF SUCCESSFUL

- Create new “Base Technologies” that enable 24-hour, **autonomous** design
  - Extreme partitioning (bite-sized problems)
  - Parallel search and optimization
  - Machine learning: models of tools, designs
- New paradigm for design tools and methods: autonomy first
- Bring down barriers → democratize HW design

# IMPACT ON DESIGN COST

- Embedded vision chips (28nm/16nm) from Michigan Internal Design Advisors team
- Layout @Michigan: 10+ weeks, significant resource
- OpenROAD and IDEA goal: 1 day, no humans (!)



# SWINGING FOR THE FENCES

- Must achieve critical mass and critical quality









11 of 13 IDEA TA-1 subtasks

+ Base Technologies, Design

| | | |
|---|---|---|
| **Common Infrastructure** | ~~Databases / Processing~~ | |
| | ✓ Cloud Infrastructure | BROWN |
| | ✓ Timing Analysis | UCSD |
| | ✓ Parasitic Extraction | UNIVERSITY OF MINNESOTA |
| | ✓ Readers + Writers | UTD |
| | ✓ Power and SI Analysis | UNIVERSITY OF MINNESOTA |
| **Layout Generators** | ✓ Logic Synthesis | BROWN |
| | ✓ Floorplanning | ILLINOIS |
| | ✓ Placement | UTD, UCSD |
| | ✓ Clock Tree Synthesis | UCSD |
| | ✓ Detailed Routing | UTD, ILLINOIS |
| | ✓ Layout Finishing | UTD, UCSD |
| **Design** | ~~SoC Design Advisors~~ | |

# SWINGING FOR THE FENCES

- **Internal Design** team (Michigan)
  ~70 Ph.D., 50 M.S. graduates
  + 15 new SOC designs each year



- **Tools** team (UCSD, Illinois, UMinn, UT-Dallas, Brown):
  ~150 Ph.D., 80 M.S. graduates
  + many tools, engines “on the shelf”



- **Qualcomm:** HW design, SOC-Pkg-PCB
- **Arm:** IP, system design + ML guidance



# AND MORE …

- Open-sourcing of commercial timing engine
- Donated commercial tool source code base
- Industry advisors and technical contributors
  - Dr. Chi-Ping Hsu, Avatar
  - Dr. Noel Menezes, Intel
  - Dr. Richard Ho, Google
  - …
- Worldwide outreach, engagement, support …



Parallax software

National Taiwan University

KAIST

UFRGS UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL

CUHK 香港中文大學

SEOUL NATIONAL UNIVERSITY

Google

GLOBAL FOUNDRIES

intel

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# ERI ELECTRONICS RESURGENCE INITIATIVE

## SUMMIT

**2018** | SAN FRANCISCO, CA | **JULY 23-25**