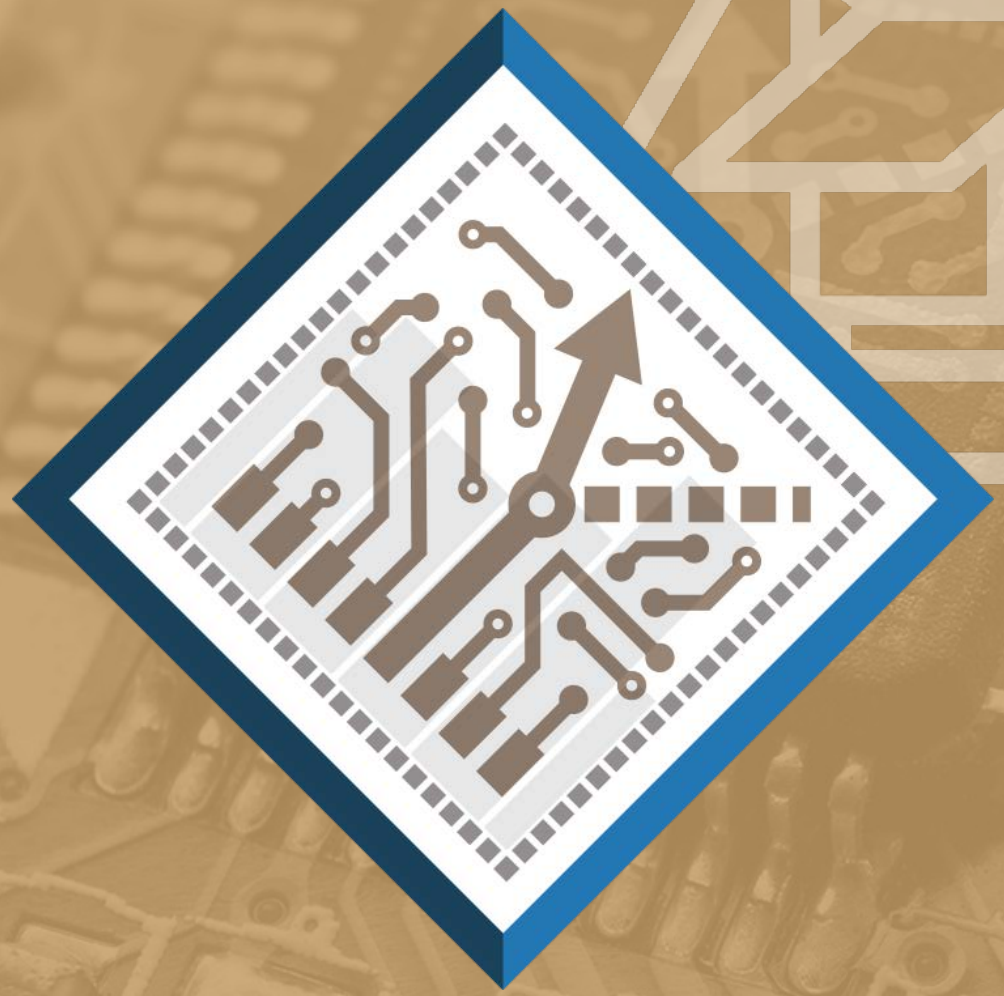
Andrew B. Kahng

UC San Diego



OpenROAD: Foundations and Realization of Open, Accessible Design

OPENROAD: NO HUMANS, 24 HOURS

IDEA will create a no-human-in-the-loop hardware compiler for translating source code to layouts of System-On-Chips, System-In-Packages, and Printed Circuit Boards in less than 24 hours

A. Olofsson, ISPD-2018 keynote

- **Traditional focus: ultimate performance, power, area**
- **Our focus: ultimate ease of use and runtime**
- **Enable access to silicon for all designers**

OPENROAD: NO HUMANS, 24 HOURS + OPEN SOURCE

IDEA will create a no-human-in-the-loop hardware compiler for translating source code to layouts of System-On-Chips, System-In-Packages, and Printed Circuit Boards in less than 24 hours

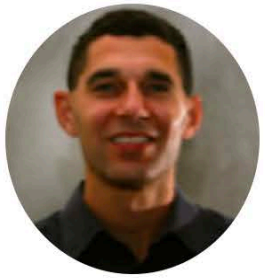
A. Olofsson, ISPD-2018 keynote

- **Digital tool flows for chip, package and board**
- **All tools open-source**
  - **Seed an ecosystem**
  - **Bring EDA research closer to industry and designers**

OPENROAD TEAM: PI'S AND FACULTY

ANDREW KAHNG*

CHUNG-KUAN CHENG



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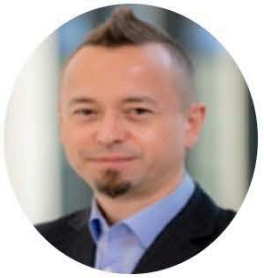
MATTEO COLTELLA*



PAUL PENZES*

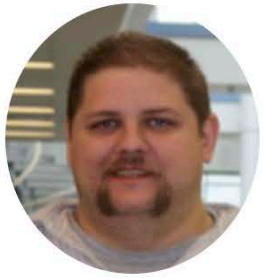
SHERIEF REDA*

UC San Diego

Arm Qualcomm Brown U.

DAVID BLAAUW

DENNIS SYLVESTER*



RONALD DRESLINSKI

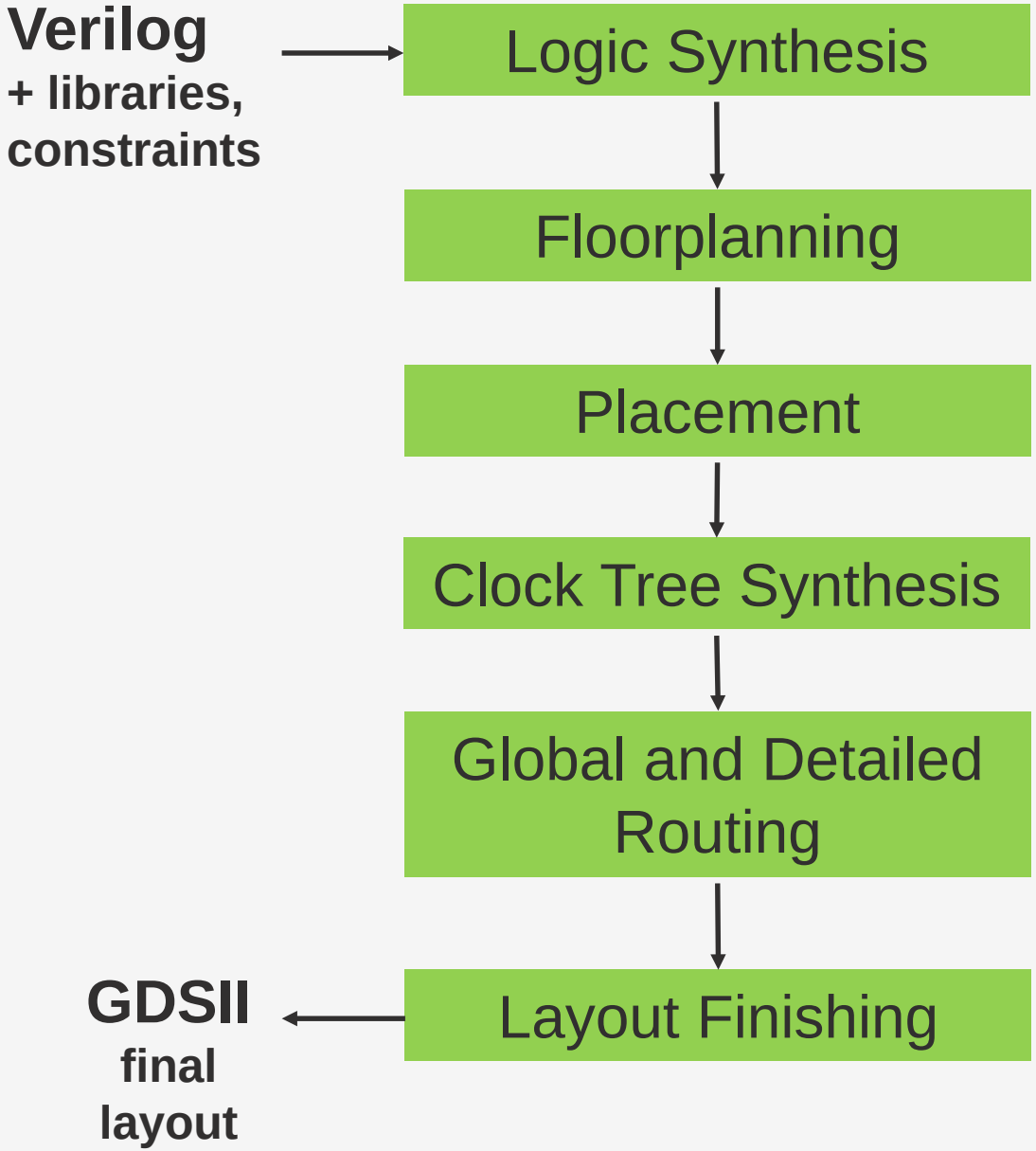
SACHIN SAPATNEKAR*

CARL SECHEN*

BILL SWARTZ

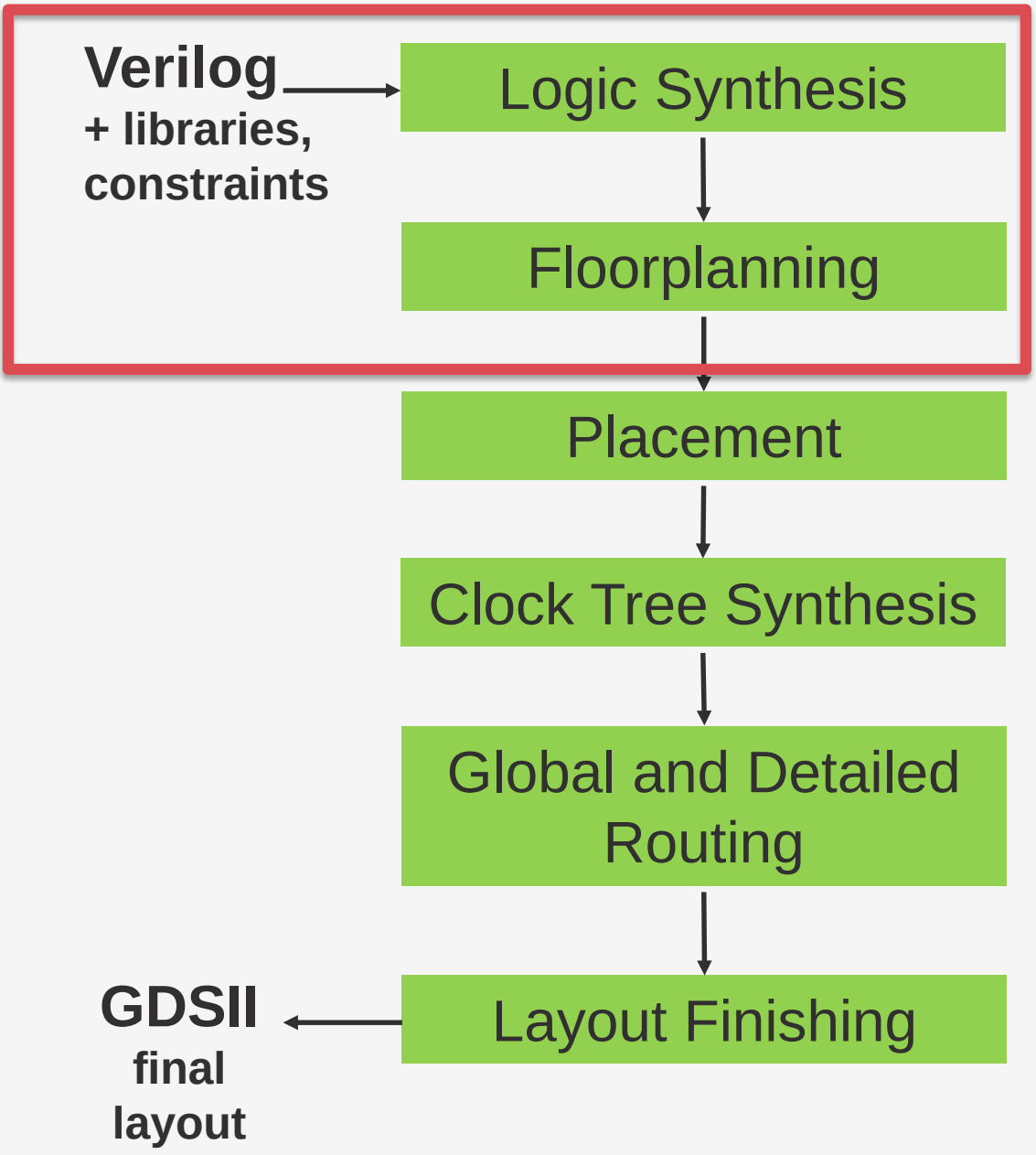
University of Michigan U. Minnesota UT Dallas

INITIAL FOCUS ON DIGITAL IC: "RTL TO GDS"



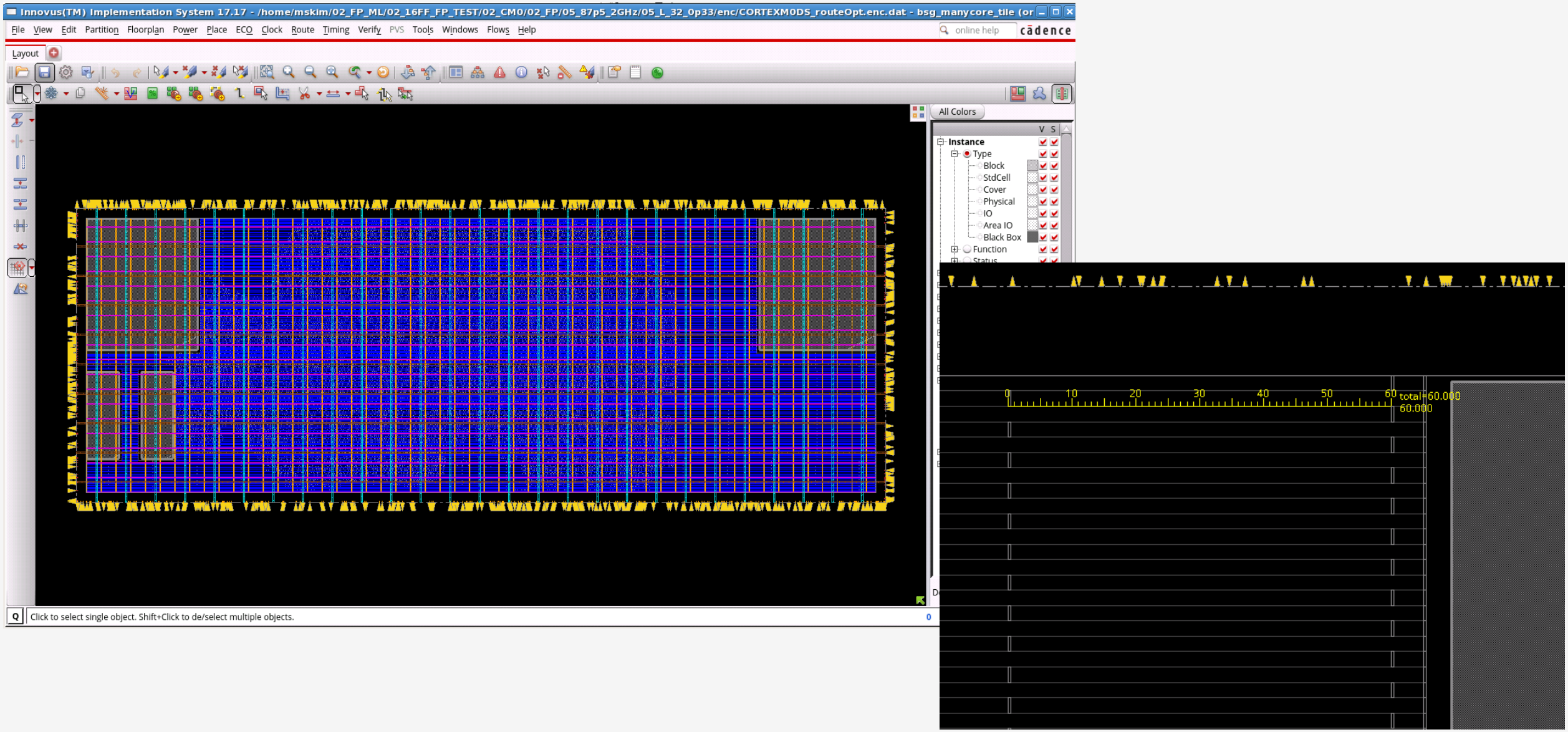
- **Demonstration: DRC-clean RTL-to-GDS capability: push-button in foundry enablement**
  - Key first step in a 4-year journey
- **Test platform: RISC-V based core from U. Michigan, "VanillaBean"**
  - **In SOC tapeouts from 16nm to 180nm**
  - **17K standard-cell instances**
  - **66K bits of SRAM**
- **TSMC 65LP technology**

SYNTHESIS AND FLOORPLANNING

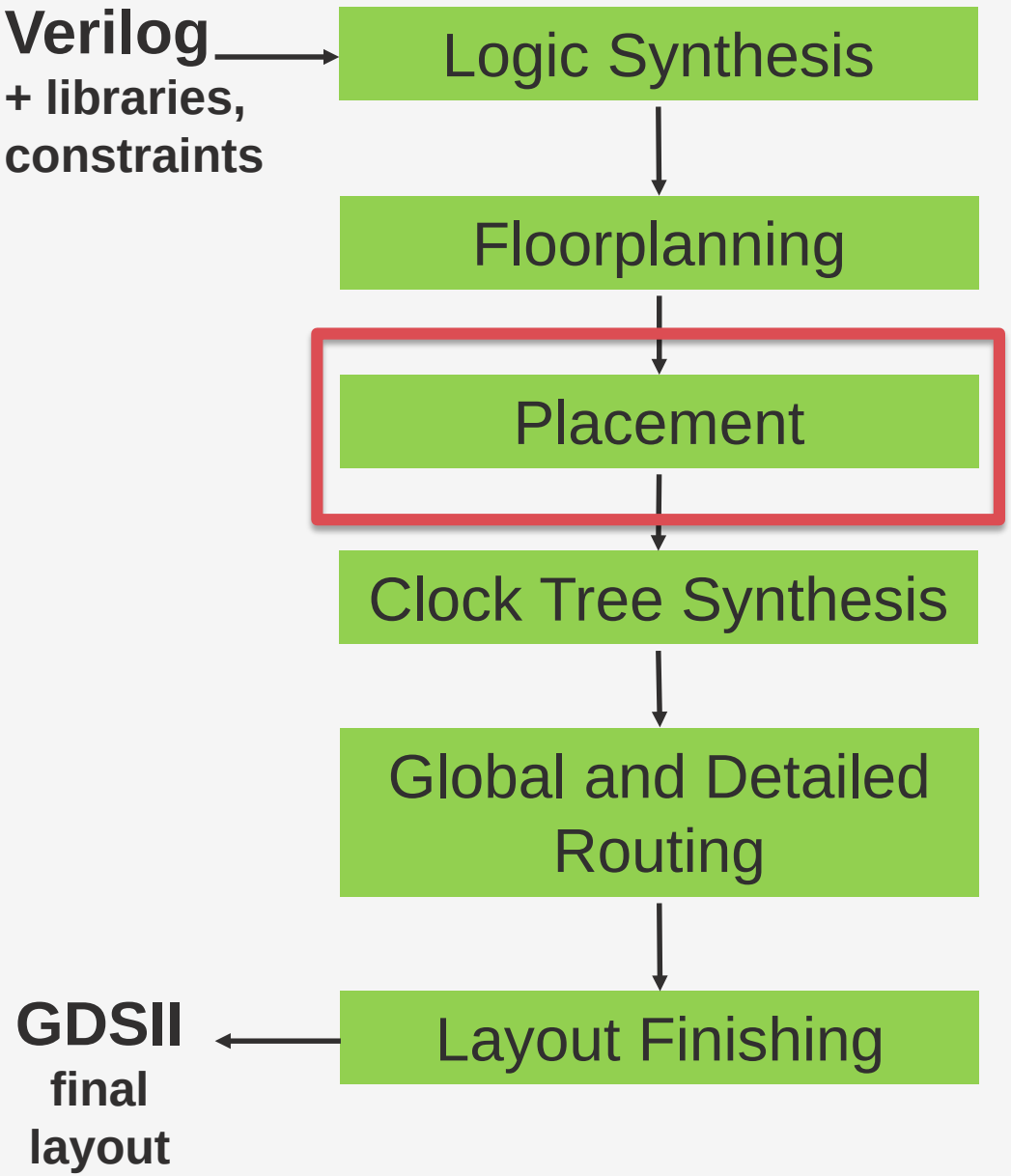


- **Logic synthesis** Brown U.
  - Based on Yosys+ABC, with many extensions (e.g., for timing correctness)
  - Outputs structural Verilog netlist
- **Floorplanning** Parallax, UCSD, Arm
  - Verilog to .def initialized floorplan
  - IO placement UFRGS (Brazil)
  - Analytic placement of blocks + cells
  - Macro block packing
  - P/G mesh generation
  - Well tap insertion

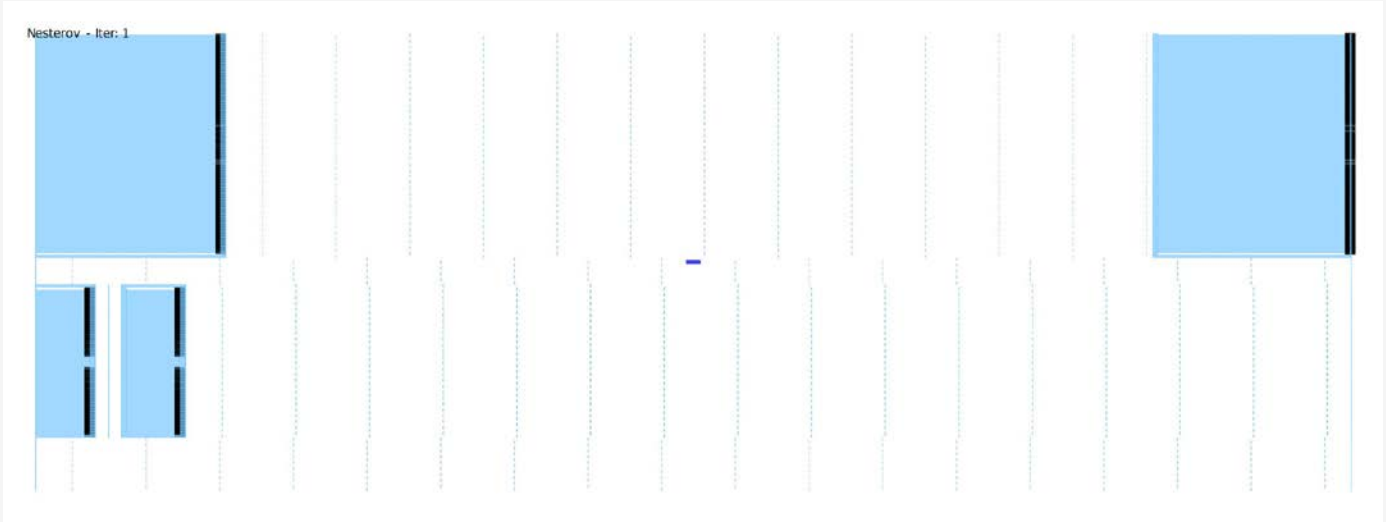
FLOORPLANNING OUTPUT



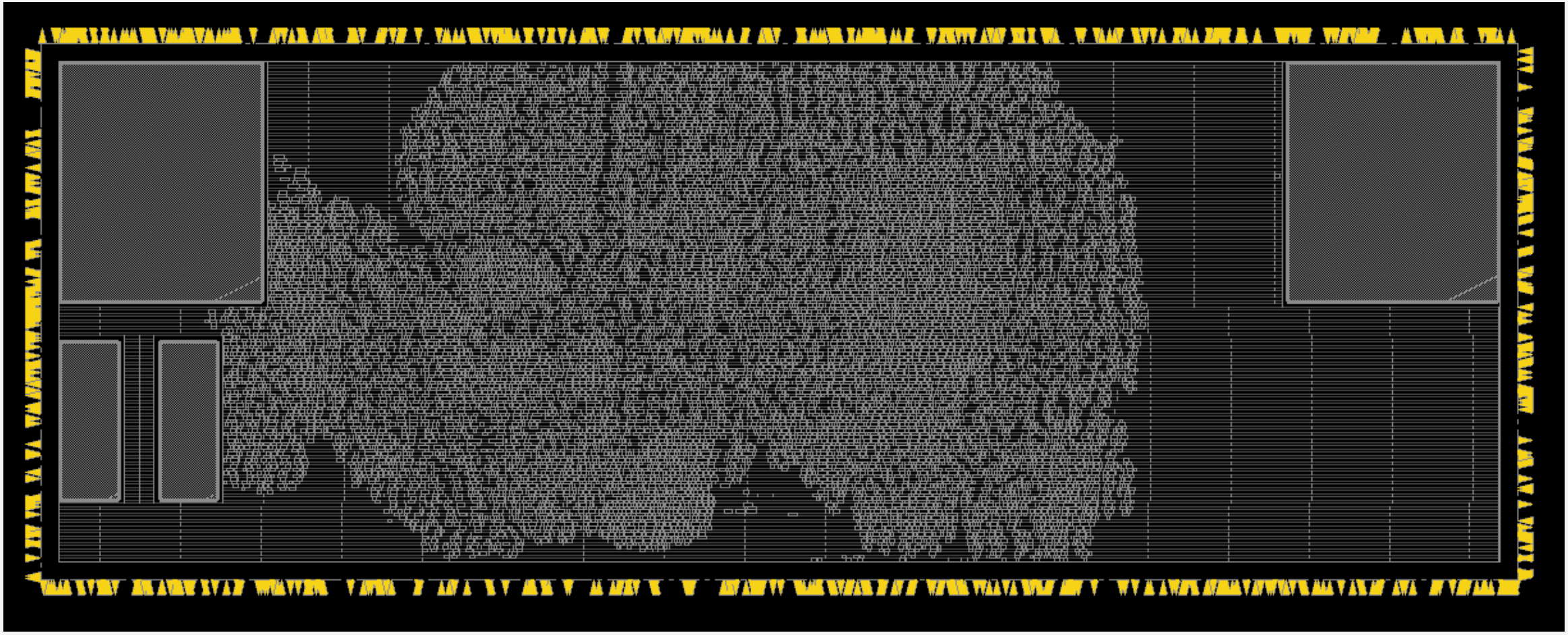
PLACEMENT



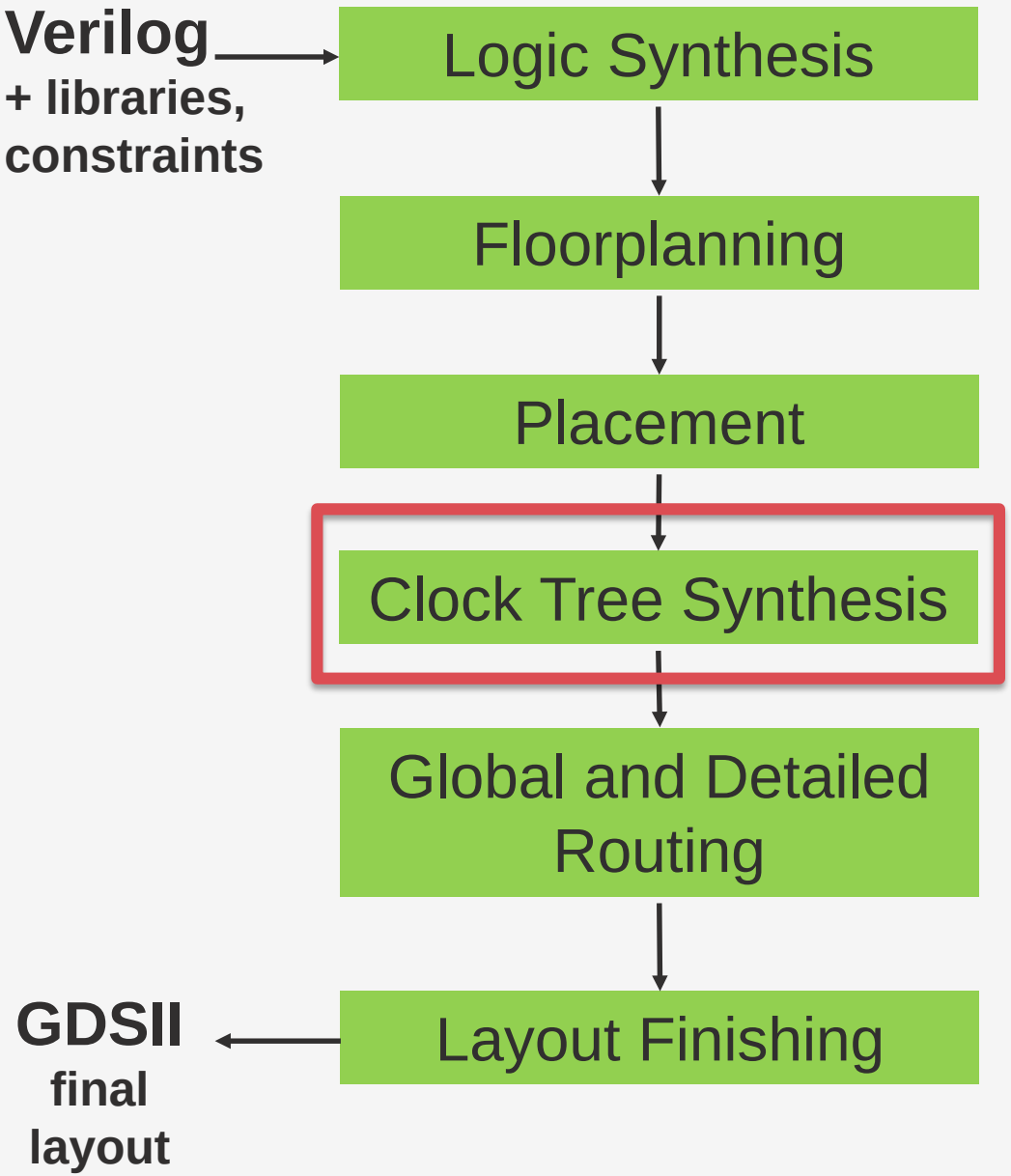
- **Placement** UCSD
  - Timing-driven
  - Mixed-size (macros + cells)
  - Electrostatics-based analytic approach
  - Sizing and buffering: Resizer Parallax
  - Legalization step: OpenDP POSTECH (Korea)



PLACEMENT OUTPUT

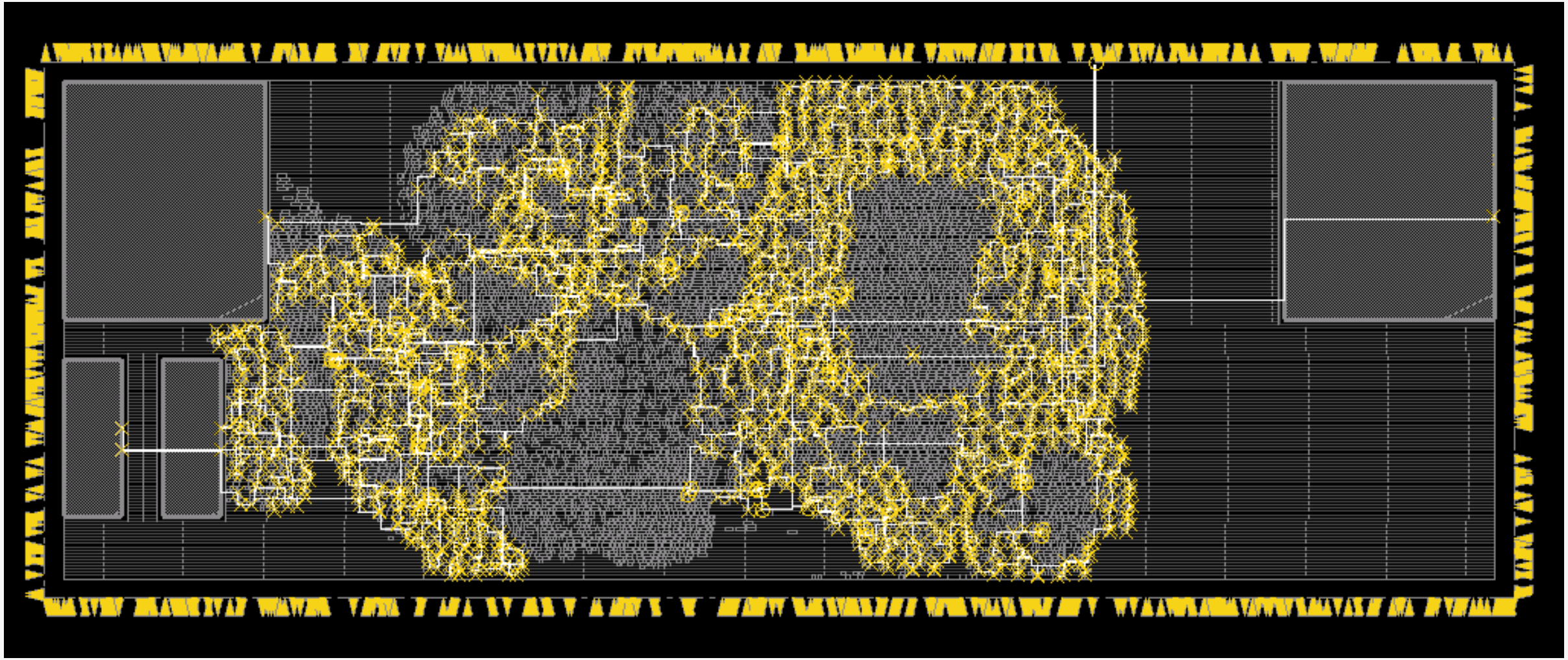


CLOCK TREE SYNTHESIS

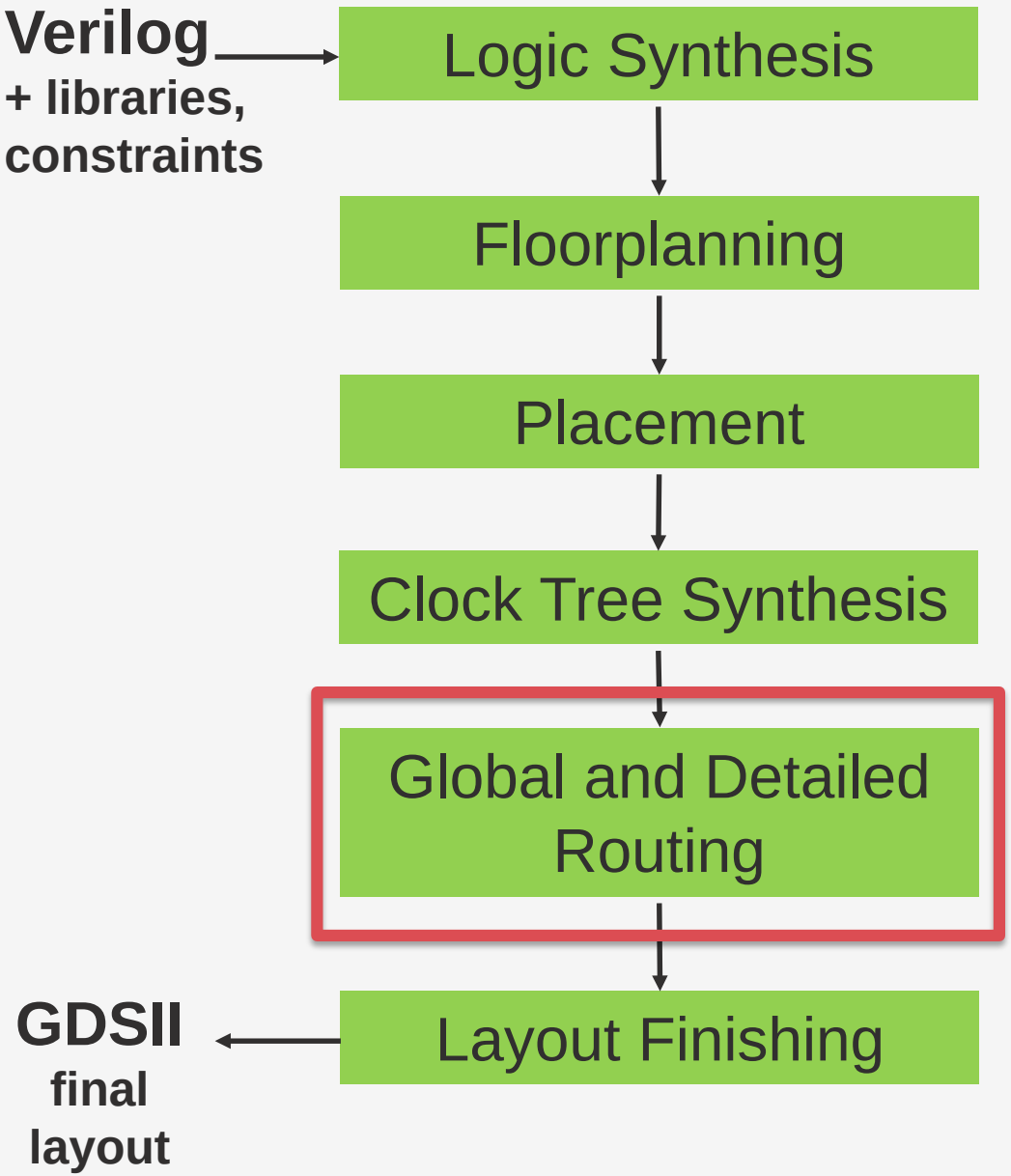


- **Clock Tree Synthesis** UCSD
  - "Generalized H-Tree" approach implemented with Qualcomm guidance
  - Dynamic programming for tree topology generation
  - Minimum-cost flow for clustering and buffer location
  - One-time technology, library characterization step

CLOCK TREE SYNTHESIS OUTPUT

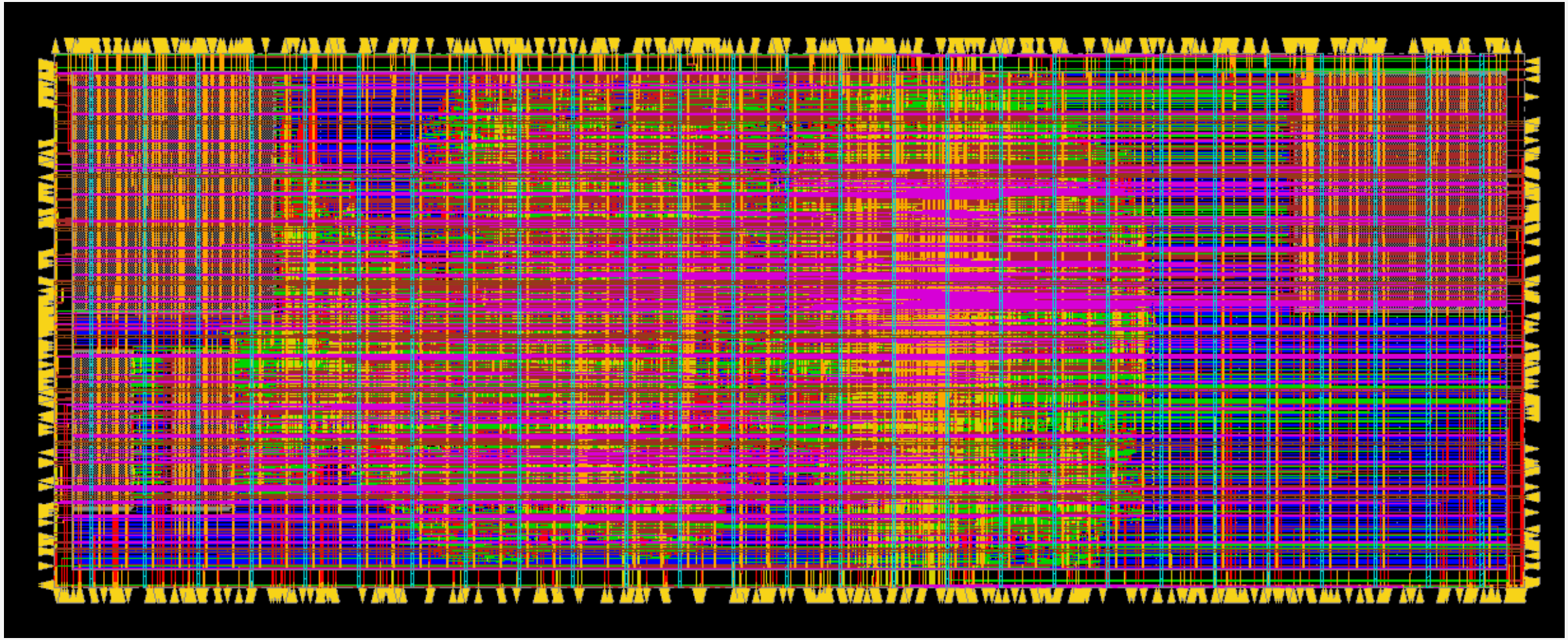


GLOBAL AND DETAILED ROUTING



- **Global Routing** UT-Dallas
  - Starting point: UT-Austin "BoxRouter 2.0"
  - Mathematical programming-based approach
  - "Route guide" output as interface to detailed routing
- **Detailed Routing** UCSD
  - DRC-correct in 65nm commercial foundry enablement
  - First-ever in academia

DETAILED ROUTING OUTPUT



VERIFY DRC: 0 VIOLATIONS

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VERIFY DRC ..... Sub-Area: {679.680 161.280 764.640 241.920} 35 of 65  Thread : 5
VERIFY DRC ..... Sub-Area: {764.640 0.000 849.600 80.640} 10 of 65  Thread : 6
VERIFY DRC ..... Sub-Area: {84.960 241.920 169.920 322.560} 41 of 65  Thread : 6
VERIFY DRC ..... Sub-Area: {84.960 80.640 169.920 161.280} 15 of 65  Thread : 3
VERIFY DRC ..... Sub-Area: {424.800 0.000 509.760 80.640} 6 of 65  Thread : 2
VERIFY DRC ..... Sub-Area: {594.720 0.000 679.680 80.640} 8 of 65  Thread : 7
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VERIFY DRC ..... Thread : 6 finished.
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 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:04.5  ELAPSED TIME: 1.00  MEM: 2.0M) ***

innovus 1> win
innovus 2>
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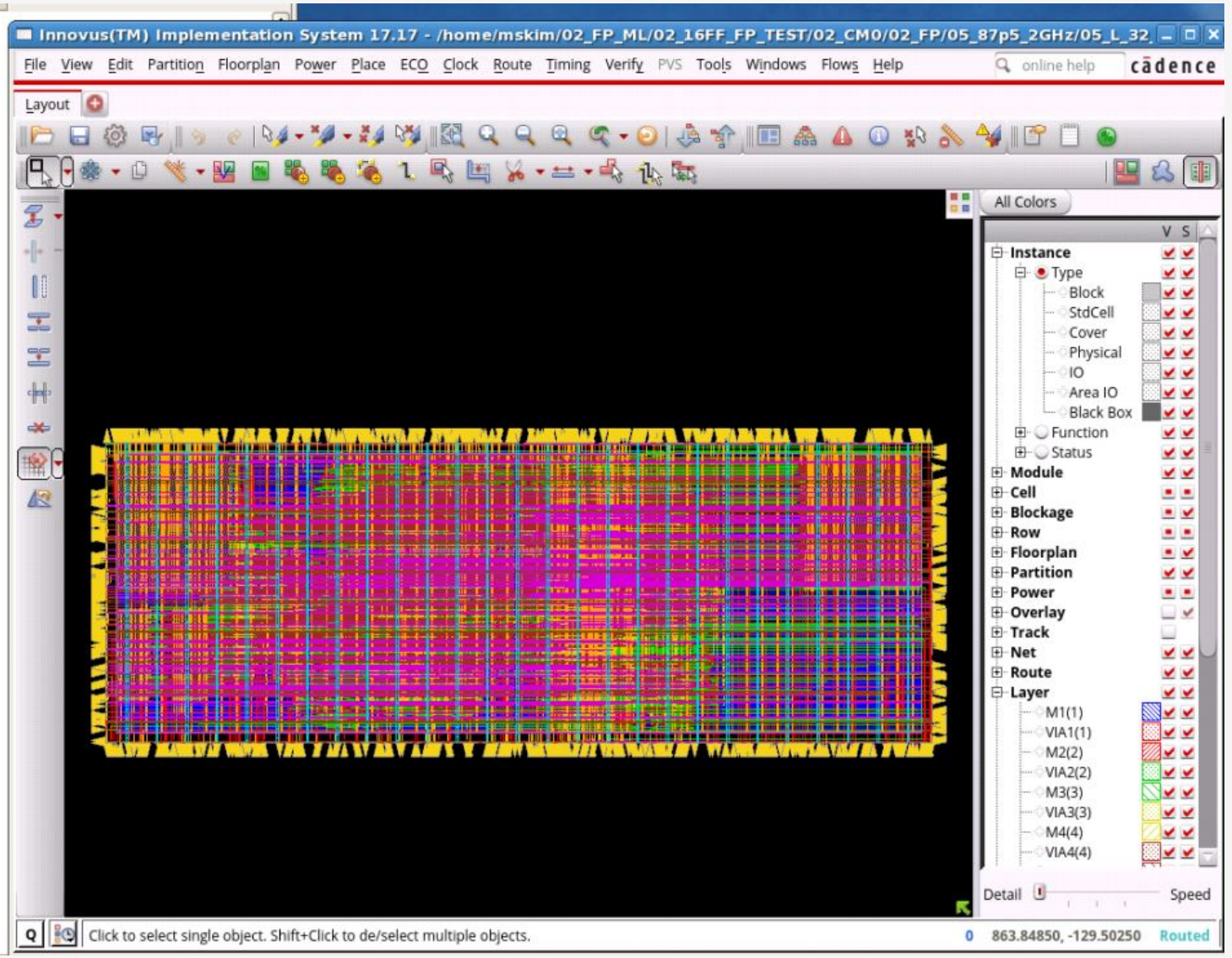
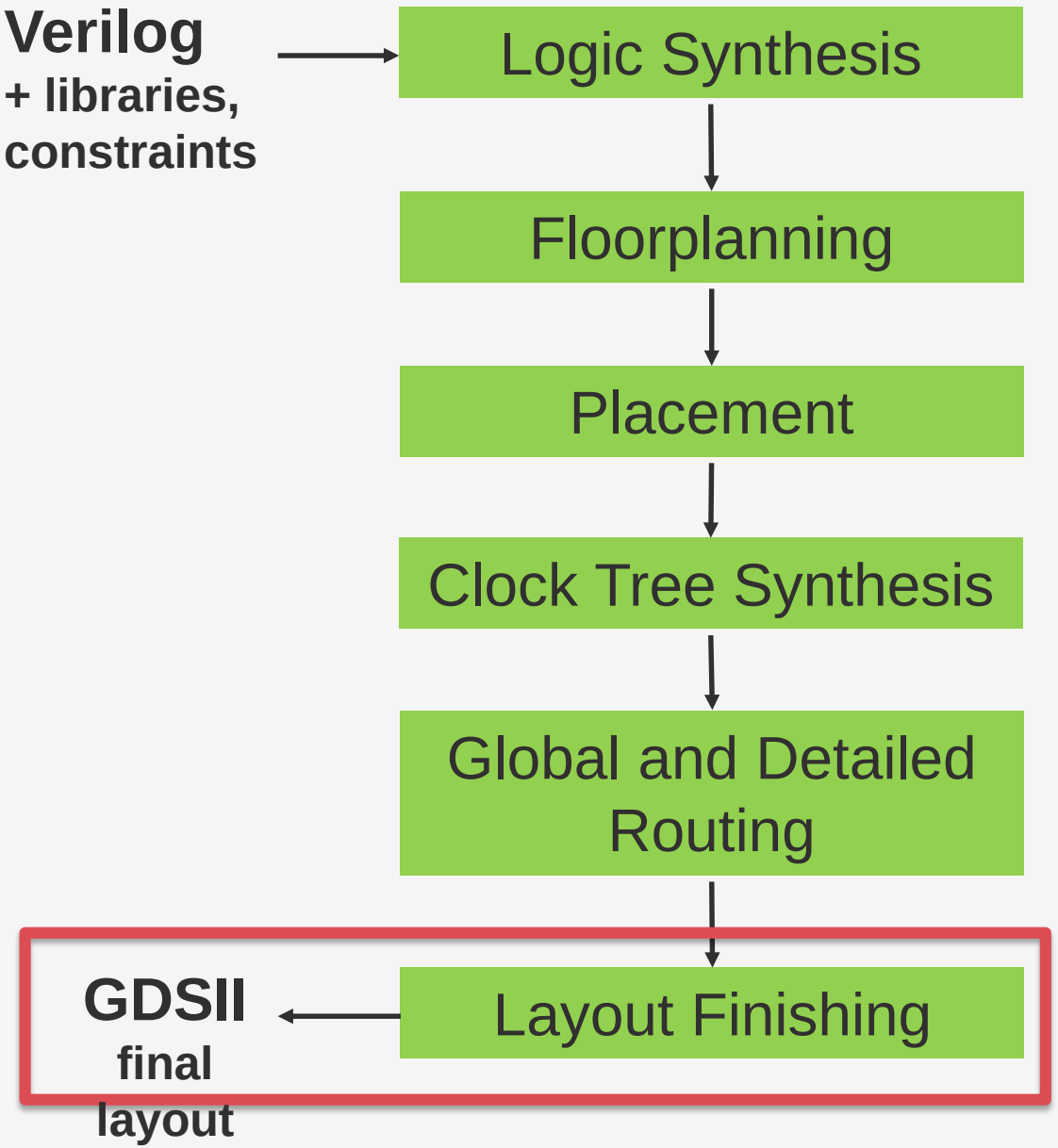


LAYOUT FINISHING (GDS OUT)

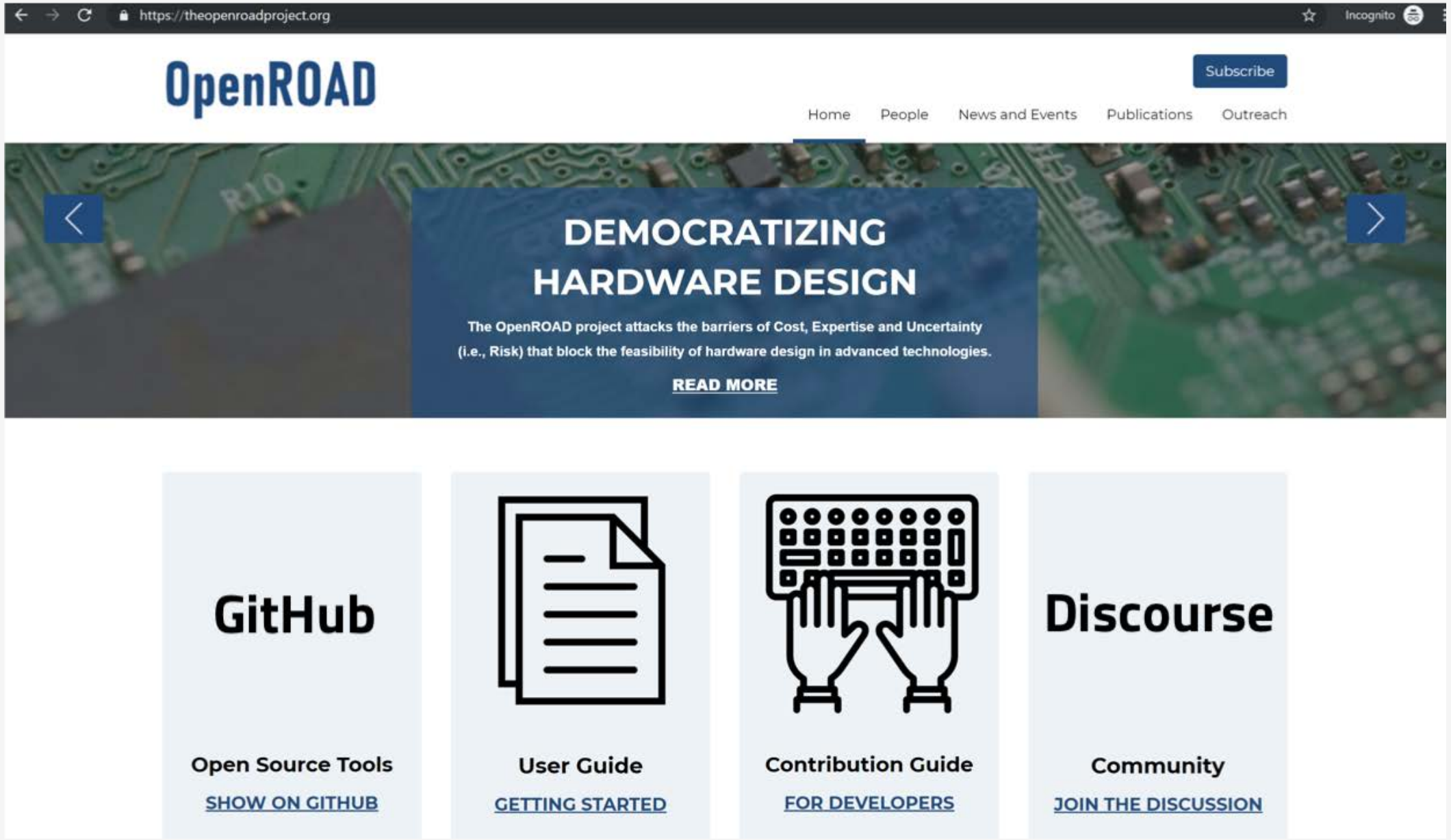


- **Routed .def to merged .gds accomplished using Magic**
- **Generous collaboration from Tim Edwards of efabless.com**

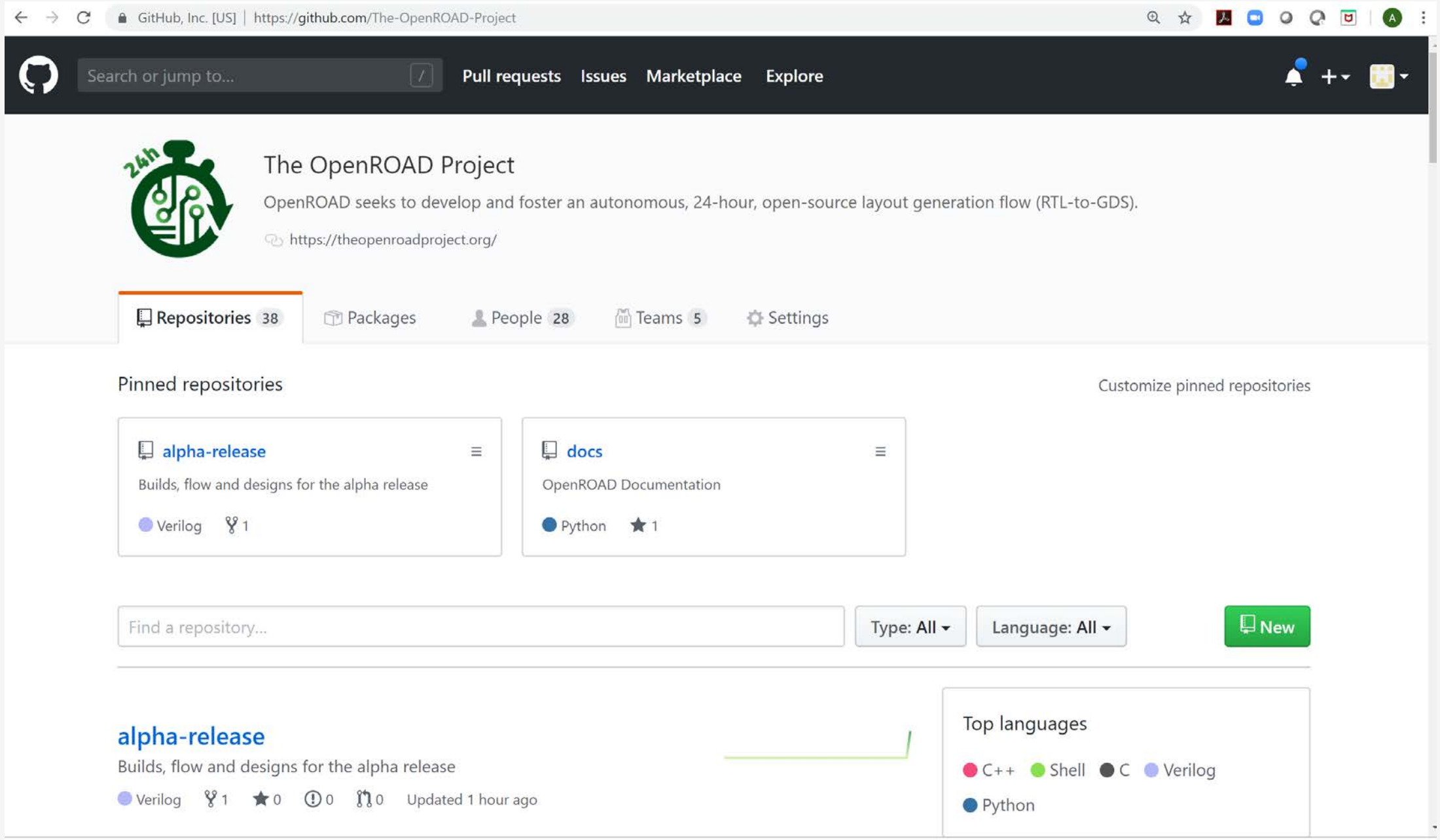
LOOKING TOWARD OPENROAD V1.0 (JULY 2020)

- **EDA industry learning curve: architecture of synthesis, place & route**
  - **1980s: file-based integration** **tool chain** ("Alpha", July 2019)
  - **2000s: tightly coupled algorithms on a shared incremental substrate**
    tight integration (v1.0, July 2020) → implies first-ever shared DB layer in permissive open source!
- **Critical foundations: architecture, devops, database, CAE/PE**
  - **Tom Spyrou: Well known EDA system architect, OpenAccess database, PrimeTime**
    - ***Full-time in San Diego; chief architect / technical project manager***
  - **Lukas van Ginneken: Magma co-founder, synthesis and optimization**
  - **James Cherry: Pearl and Parallax static timing engines**

WEBSITE: THEOPENROADPROJECT.ORG



GITHUB.COM/THE-OPENROAD-PROJECT



THEOPENROADPROJECT.ORG/OUR-TEAM/

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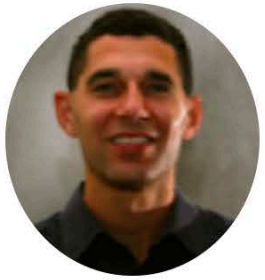

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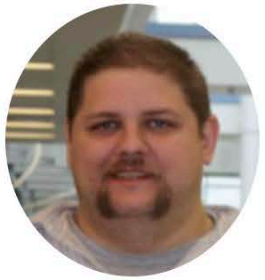

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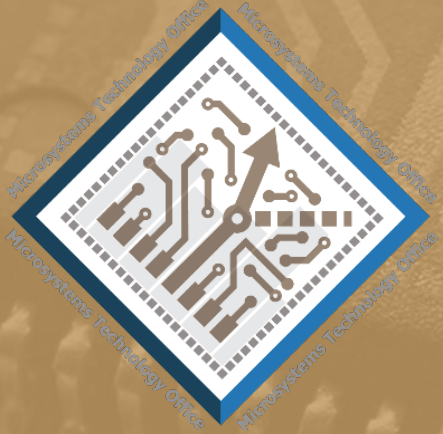

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