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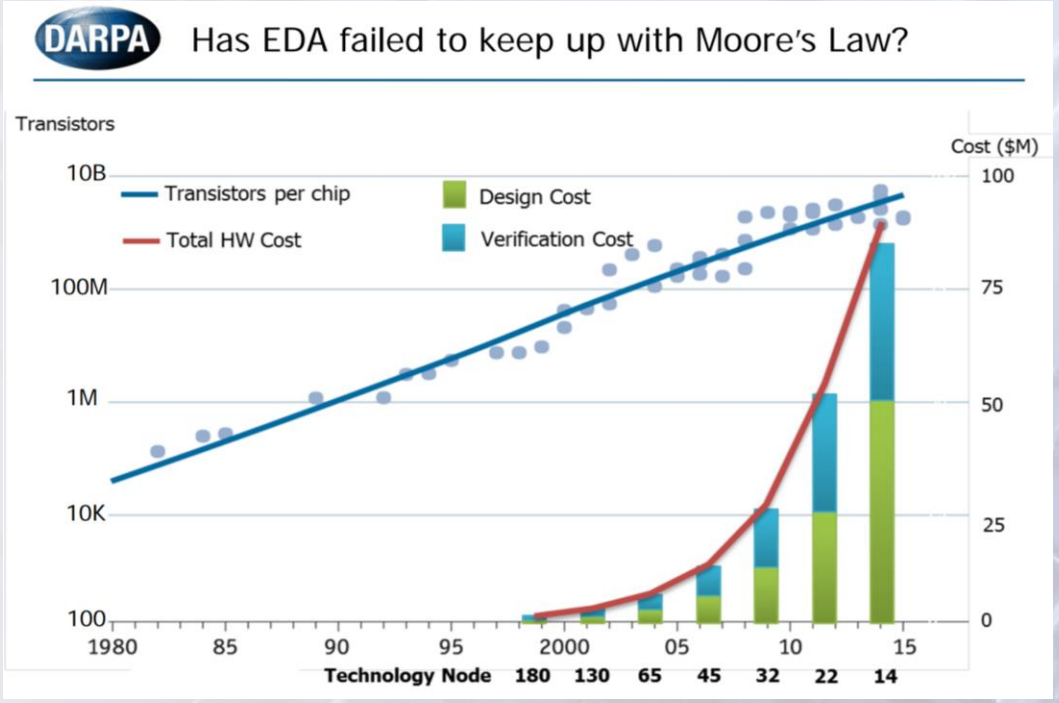
OPENROAD:

FOUNDATIONS AND REALIZATION OF OPEN, ACCESSIBLE DESIGN

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

THE CRISIS OF HARDWARE DESIGN…

- ASIC design in advanced technologies: Huge barriers of Cost, Expertise and Risk



Source: http://www.ispd.cc/slides/2018/k2.pdf

...IS A CRISIS OF INNOVATION

- Hardware innovators actually write code !
  - VHDL or Verilog that gets compiled into ICs

- **The Real Crisis:** Innovators are unable to evaluate their code in terms of SWaP and performance metrics

- **Root Cause: The Crisis of Hardware Design**

HOW IS ASIC DESIGN DONE TODAY?

- Very sophisticated tools with 1000s of commands
- Tool supplier focus: ultimate performance, power, area
- Large teams of expert users, many manual steps
- Long project schedules
- Significant project risks

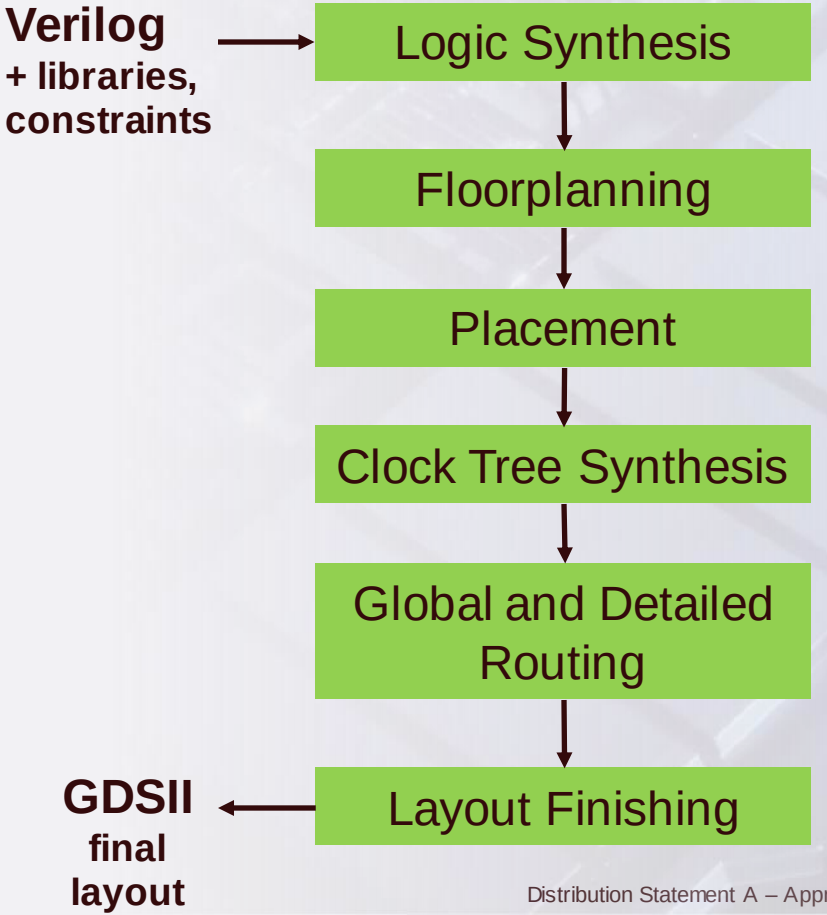
OPENROAD: NO HUMANS, 24 HOURS

- FOCUS: ULTIMATE ease of use and runtime

- Directly attack the crises of design and innovation
  - Schedule barrier: RTL-to-GDS in 24 hours
  - Expertise barrier: No-human-in-the-loop, tapeout GDS
  - Cost barrier: Open source (and runs in 24 hours)

- Unleash system innovation and design innovation
- Enable tool customization to system, application needs

OPENROAD V1.0



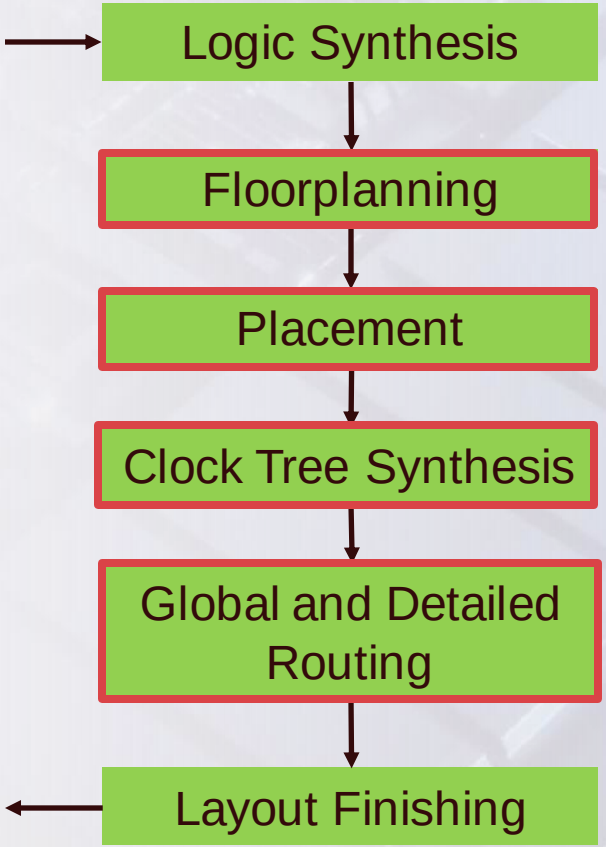
- **ERI 2019: Proof of capability**
  - **DRC-clean RTL-to-GDS, 65nm**
  - **"File-based flow" 1980's EDA**
- **Today: a v1.0 OpenROAD tool**
  - **DRC-clean RTL-to-GDS, 12nm**
  - **UW's "BlackParrot" SoC**
  - **Integrated tool, modern EDA**

OPENROAD AVAILABILITY

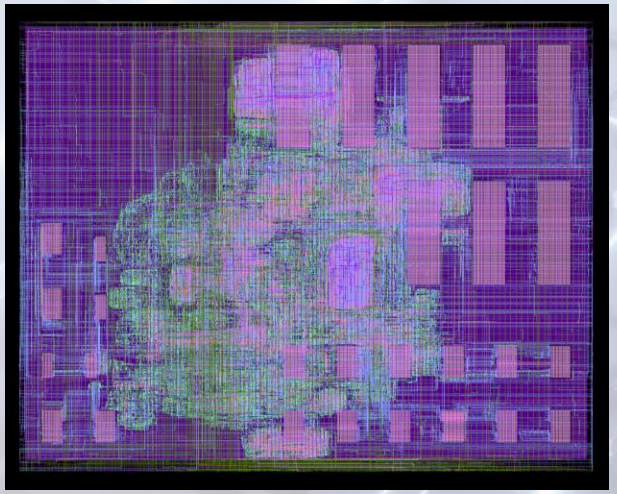
- The Project on GitHub
  - https://github.com/The-OpenROAD-Project
- The Flow, developed by internal design advisors subteam
  - Drives the entire automation of the full flow using tool components focused on automation
  - https://github.com/The-OpenROAD-Project/OpenROAD-flow
- The Top-level Application
  - An integrated EDA tool focused on full automation
  - https://github.com/The-OpenROAD-Project/OpenROAD

OPENROAD V1.0 IN ACTION

Verilog
+ libraries, constraints

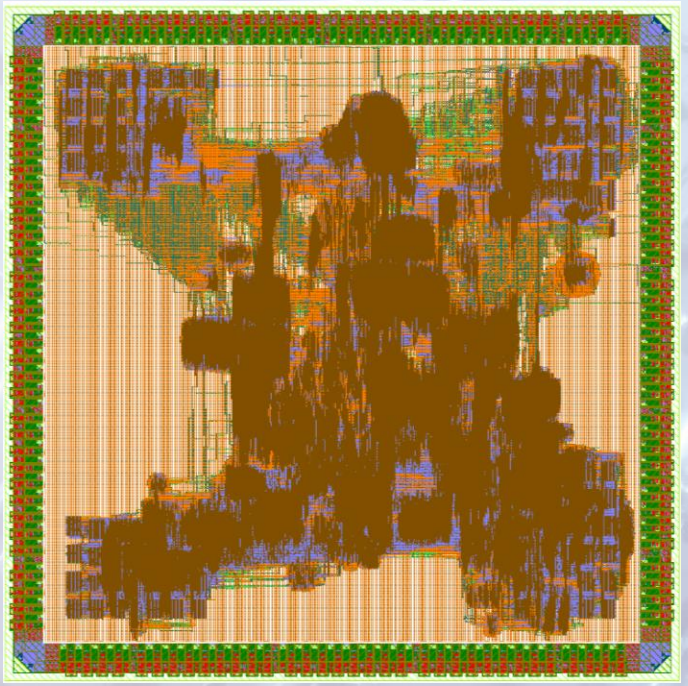


GDSII
final layout



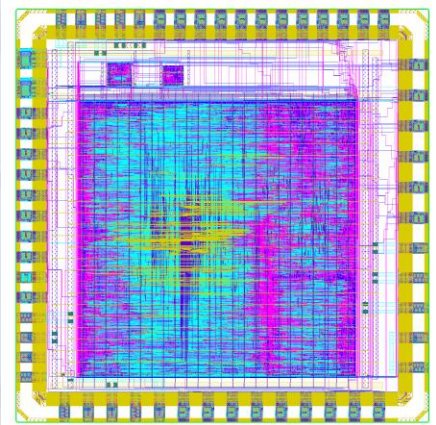
12NM SOC TAPE-IN: BLACKPARROT

- U. Washington RISC-V SoC
  - 2 cores, 700K cells, 98 macros
  - 3mm x 3mm package
- GLOBALFOUNDRIES 12LP PDK
  - Invecas IOs
  - Arm standard cells and RAMs
- Output GDS is DRC/LVS clean
  - Mentor Calibre w/ foundry scripts
- RTL to GDS: < 16 hours

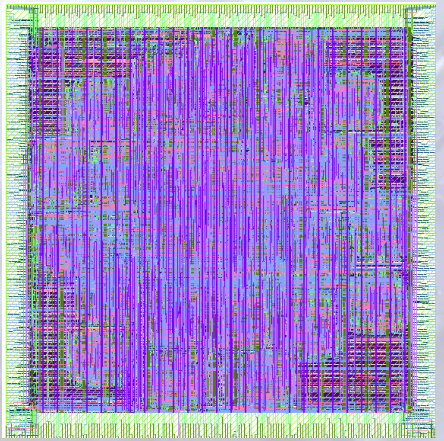


OTHER USAGE

- efabless “striVe” SOC
  - SKY130 tapeouts
  - 6 weeks → 6 hours



- ASSURE (NYU, POLIMI) obfuscated RTL
  - OpenROAD worked out of box
  - 12nm overhead: < 10%



Source: https://www.youtube.com/watch?v=EczW2IWdnOM

MANY BREAKTHROUGHS

- 12nm tapeout-capable tool from an academic research project
- Integrated architecture, database, timing engine – built to last
- Many academic firsts
  - Floorplanner
  - Detailed router
  - No-humans, 24-hours, DRC-clean
- Foundation for research, innovation, transitions

PHASE 2: GROWTH + TRANSITIONS

- Growing the sustainable business + research ecosystem
  - Businesses will productize, distribute, support
  - Research ecosystem will innovate – faster
  - Special application, system needs will be better served
- Growing the technology
  - 7nm capability
  - Machine learning → intelligence and self-adaptation
  - Cloud deployment → exploiting more threads in 24 hrs
- Growing the user and developer community

OPENROAD TEAM: PI'S AND FACULTY

Kahng

Cheng

Saul

University of California, San Diego

Coltella

Arm

Penzes

Qualcomm

Blaauw

Sylvester

Dreslinski

University of Michigan

Sapatnekar

Reda

University of Minnesota

Brown University

GLOSSARY

- ASIC – Application-Specific Integrated Circuit
- DRC – Design Rule Check
- EDA – Electronic Design Automation
- GDS – Graphic Design System (also GDSII)
- LVS – Layout Versus Schematic
- PDK – Process Design Kit
- RAM – Random Access Memory
- RISC – Reduced Instruction-Set Computer
- RTL – Register-Transfer Level
- SoC – System-on-Chip
- SWaP – Size, Weight and Power
- VHDL – VHSIC Hardware Description Language